Harmonic Optimization of Cascade Multilevel Inverter with Unequal DC Sources

M.Periasamy[1], G.Chandran [2,] G.P.Aarthi[3]
HOD[1], Lecturer[2], Lecturer[3], Department of Electrical and Electronics Engineering,
Kongu Polytechnic College, Erode, TamilNadu
Email Id: msamyice28@gmail.com, geturchandru@gmail.com, aarthigp.ped@gmail.com

Abstract: Multilevel inverter have been attracting increasing interest recently due to the increased power rating, improving harmonic performance, and reduced electromagnetic inference (EMI) emission. A voltage source inverter is commonly used to supply a variable frequency variable voltage to a three phase induction motor in a variable speed application. The output voltage contains harmonics the different type of harmonics elimination methods are available. But all the methods have some limitations. This project deals with how to reduce the particular harmonics in the output voltage of inverter. The concept of the harmonic stepped waveform technique for the multilevel inverter is to be presented. By applying this concept, selected harmonic can be eliminated, and the output voltage THD can be improved. A procedure to achieve the appropriate switching angle is to be proposed. The proposed project is to be simulated by using MATLAB and the results are to be compared with experimental setup. The AT mega Microcontroller is to be used for generating required pulses to the cascaded multilevel inverter.

Index Terms: Multilevel Inverter, Genetic Algorithm (GA), Selective Harmonic Elimination (SHE), Micro Controller, MATLAB.

1 INTRODUCTION

Several topologies for multilevel inverts have been proposed over the years the most popular being the diode clamped, flying capacitor and cascaded H-bridge structures. One aspect which sets the cascaded H-bridge apart from other multilevel inverts is the capability of utilizing different DC voltages on the individual H-bridge cell which results in splitting the power conversion amongst higher-voltage lower-frequency and lower-voltage higher frequency inverts.

An alternate method of cascading inverts involves series connection of two three phase inverters through the neutral point of the load. An advantage of this approach is that isolated sources are not required for each phase. It should be noted that cascaded inverter system can be considered from a number of different viewpoints. Considering the cascaded inverter to be one unit, it can be seen that a higher number of voltage levels are available for a given number of semiconductor devices. Capacitors batteries and or renewable energy voltage sources can be used as a DC unequal voltage sources.

2 STAGES OF MULTILEVEL INVERTER

The three stages of CMLI are high-voltage stage, medium voltage stage and low voltage stage. The high, medium and low voltage stages are made of three-level inverters constructed using cascaded H-bridge. This method is used to avoid the undesirable high switching frequency for all the voltage stages despite the fact that the inverter's dc sources are selected to maximize the inverter levels by eliminating redundant voltage state.

3 MULTILEVEL INVERTER TOPOLOGIES

3.1 Introduction

The multilevel voltage source inverter is recently applied in much industrial application such as AC power supplies, static VAR compensators, drive systems, etc, one of the significant advantages of multilevel configuration is the harmonic reduction in the output waveform without increasing switching frequency of decreasing the inverter power output. The output voltage waveform of a multilevel inverter is composed of the number of levels of voltages, typically obtained from capacitors voltage sources.

As the number of levels reach infinity the output THD approaches zero. The number of the achievable voltages levels, is limited by voltage unbalance problems, voltage clamping requirement, circuit layout and packaging constraints.

3.2 Types of Multilevel Inverter

There are three types of multilevel inverter namely Diode-Clamped Multilevel Inverter, Flying-Capacitor Multilevel Inverter and Cascaded-Inverters with Separated Dc Sources. Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generates voltages with stepped waveforms with less distortion, less high switching frequency, higher efficiency, lower voltage devices and better electro-magnetic compatibility. The commutation of the switches permits the addition of semiconductors must withstand only reduced voltages.

3.2.1 Diode-Clamped Multilevel Inverter (DCMLI)

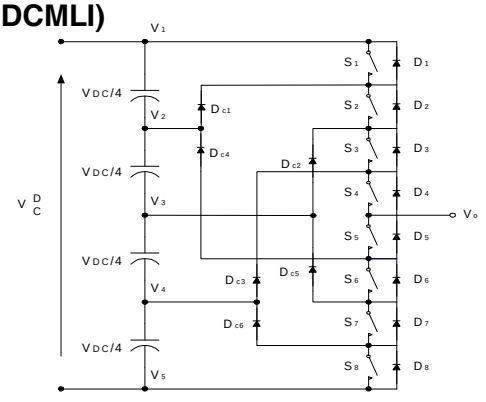


Figure 3.1: Diode-Clamped Multilevel Inverter (DCMLI)

The Diode-Clamped Multilevel Inverter uses capacitors in serried to divide up the Dc bus voltage into a set of voltage levels. To produce m level of the phase voltage, an m level diode-clamp inverter need m – 1 capacitors on the DC bus. A single phase five-level diode-clamped inverter is shown in Fig3.1.

Table 3.1: Switching Pattern of DCMLI

Power Index Value	Output Phase Voltage (V_O)				
	V1	V2	V3	V4	V5
S1	1	0	0	0	0
S2	1	1	0	0	0
S3	1	1	1	0	0
S4	1	1	1	1	0
S5	0	1	1	1	1
S6	0	0	1	1	1
S7	0	0	0	1	1
S8	0	0	0	0	1

Table 3.1 shows the phase voltage level and their corresponding switch states. When the switch is on the output voltage becomes one otherwise the value becomes zero. Table 3.1 shows the switching pattern of Diode clamped Multi- Level Inverter and the output phase voltage for the corresponding switching states when the switch S1 and S8 is ON, the output phase voltage is produced by the voltage of V_1 and V_5.

3.2.2 Flying Capacitor Multilevel Inverter

Capable of solving capacitor voltage unbalance problem and excessive diode count requirement in DCMI .Employs separate capacitors pre charged to [(nl-1)/(nl-1)x VDC], [(nl-2)/(nl-1)x VDC] ..{[nl-(nl-1)]/[nl-1]x VDC}. Size of voltage increment between two capacitors defines size of voltage steps in ICMI output voltage waveformA flying capacitor multilevel inverter in fig 2.2 uses a ladder structure of DC side capacitor where the voltage on each capacitor differs from that of the next capacitor

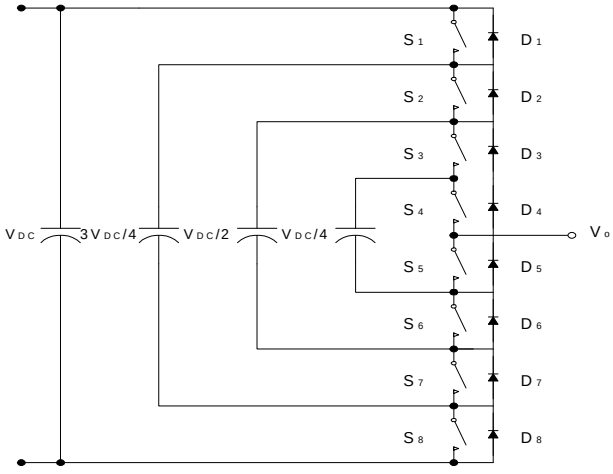


Figure 3.2: Flying Capacitor Multilevel Inverter (FCMLI)

To generate m-level staircase output voltage, m1 capacitors in the D bus are needed. Each phase-leg has an identical structure. The size of the voltage increment between two capacitors determines the size of the voltage levels in the output waveform.

Table 3.2 shows the phase voltage level and their corresponding switch states. From table 3.2, state 1 represents that the switch is on and state 0 represents the switch is off.

Table 3.2: Switching Pattern of FCMLI

Output V_{Ao}	Switch State							
	Sa1	Sa2	S_{am-1}	S_{am}	$S_{a'1}$	$S_{a'2}$	$S_{a'm-1}$	$S_{a'm}$
$V_5=V_{dc}$	1	1	1	1	0	0	0	0
$V_4=3V_{dc}/4$	1	1	1	0	1	0	0	0
$V_3=V_{dc}/2$	1	1	0	0	1	1	0	0
$V_2=V_{dc}/4$	1	0	0	0	1	1	1	0
$V_1=0$	0	0	0	0	1	1	1	1

Table 3.1 shows the phase voltage level and their corresponding switch states. V

3.2.3 Cascaded Multilevel Inverter

The general function of this multilevel inverter is the same as that of the other two previous inverters. This multilevel inverter using cascaded inverter with SDCSs synthesis a desired voltage from several independent sources DC voltages which may be obtained from batteries, fuel cells, all solar cells. of different level inverters are connected in series

A. Circuit Diagram

Figure 3.2: Cascaded Multilevel Inverter

B. Block Diagram

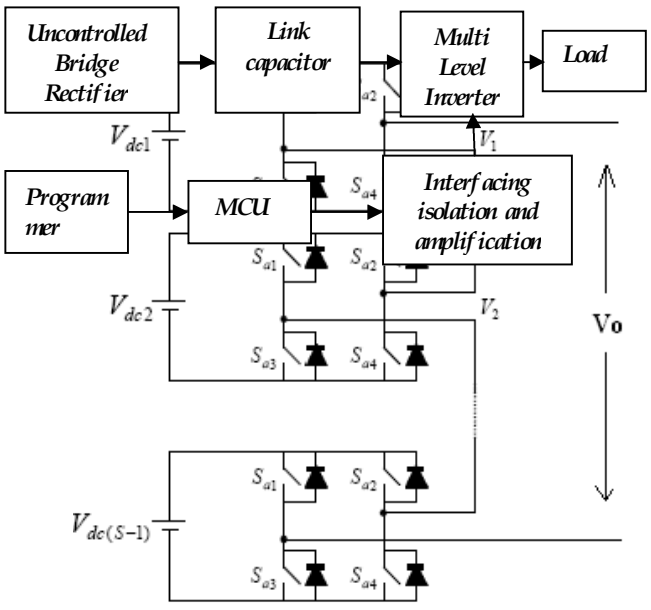


Figure 3.3 Block Diagram of CMLI

4. HARMONIC REDUCTION TECHNIQUE

4.1 Fourier Analysis.

In multilevel inverter the Fourier series is used to find the expression for output voltage. The Fourier expression for the output voltage is found because the angles are related with output voltage expression and the output voltage is quarter wave symmetry. So the Fourier series constants a_0, a_n become zero and we have to find only b_n.

$$V_o(\omega t) = \{ a_0 + S (a_n \cos n\omega t + b_n \sin n\omega t) \} \sin n\omega \quad \ldots.4.1$$

$$\text{-----} \quad N=1, 2, 3\ldots$$

The output voltage expression For five level inverter is found as

$$V_o(\omega t) = S (4Vdc/n\pi) (\cos\alpha_1 + \cos\alpha_2 + \cos\alpha_3 + \cos\alpha_4) \sin n\omega t \quad .4.2$$

$$n = 1, 3, 5\bullet\bullet\bullet$$

4.2 Harmonic Analysis

The proposed system analyses the frequency spectrum and Voltage control. In conduction angle control the lower order harmonics are reduced. By adjusting the turn on angle to various levels, it is possible to reduce the lower order harmonics. And the efficiency, power factor is improved. The Fourier expression is also obtained for the output voltage of five-level inverter.

4.3 Simulation circuit

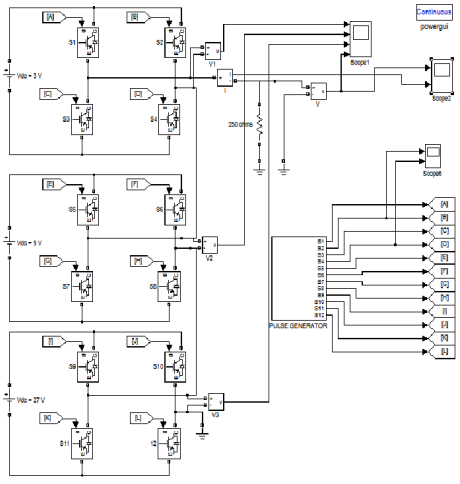


Figure: 4.1 Simulink Models of 27 Levels CMLI

ig 4.3 shows MATLAB model of model three stage cascaded multilevel inverter with modulation control. This model contains DC source voltages, gate pulse circuit, power switches like IGBT's.

4.3.1. Simulation Pulse Output

Figure 4.2.SPWM- P7, P8, P9, P10, P11, P12 pulses

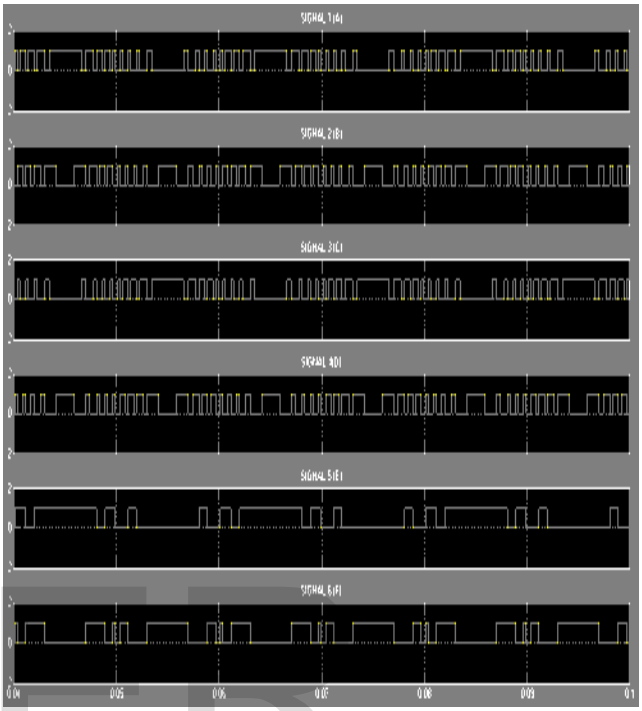
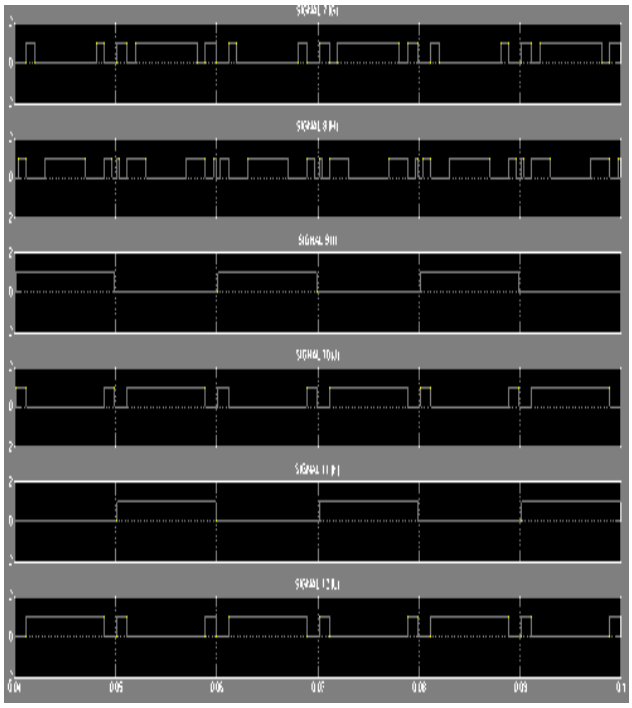
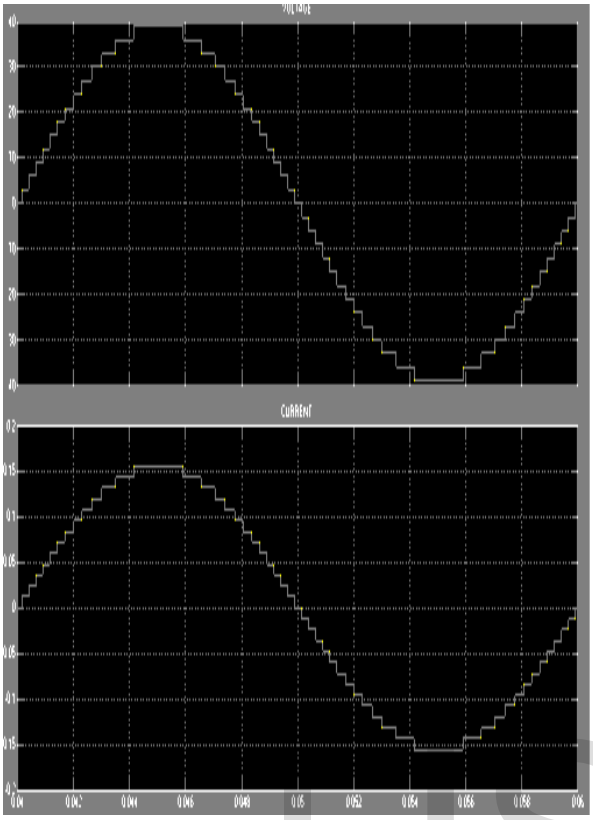


Figure 4.3. SPWM- P7, P8, P9, P10, P11, P12 pulses



4.3.3. Simulation Output for 27 Levels

Figure 44. Output of 27 levels CMLI



4.4 Hardware Output

4.4.1. Genetic Algorithms

```
% A Program For Analysis of Sinusoidal Pulse Width Modulation Of An AC
% Signal.% PART I (preparation)
% In this part the screen is cleared, any other functions, figures and
% variables are also cleared. The name of the programm is displayed.
clc
Clear all
disp('Sinusoidal Pulse Width Modulation of AC Signal')
disp(' ')
% In this part the already known variables are entered, the user is
% asked to enter the other variables.
% Vrin is the rms value of the input supply voltage in per unit.
Vrin=1;
% f is the frequency of the input supply voltage.
```

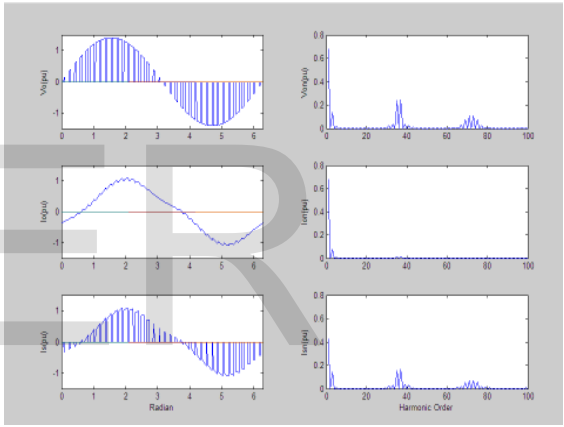
Sinusoidal Pulse Width Modulation of AC Signal
The frequency of the input supply voltage, f = 50
The modulation index, ma, (0<ma<1), ma = 0.1
The phase angle of the load in degrees = 30
The number of pulses per half period = 12
Answer

Alpha	Beta	Width
7.3500	7.6500	0.3000
22.2000	22.8000	0.6000
37.0500	37.9500	0.9000
51.9000	53.1000	1.2000

The rms Value of the Output Voltage,
Vo = 0.2828
The rms Value of the output voltage fundamental component Vrms = 0.0799
The RMS value of the load current is
CORMS = 0.0812
The RMS value of the supply current is
CSRMS = 0.0217
Performance parameters are
THD Vo = 3.3924
THD Io = 0.1760
THDIS = 3.6124
PF = 0.0796

4.4.2. Harmonic Order

Figure 45 Harmonic Order



4.4.3. Generation of the output Voltage pulses

Figure 46 Generation of the output Voltage pulses

4.4.4. MATLAB Model for 11 Levels CMLI

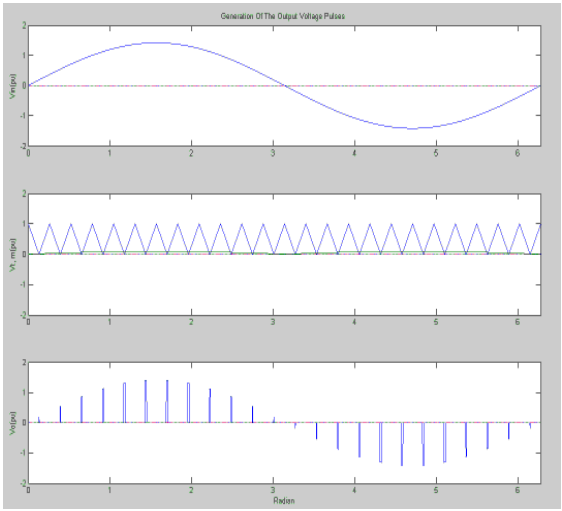
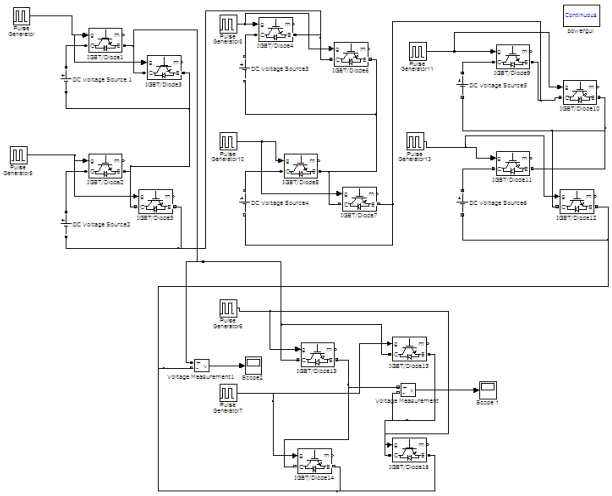
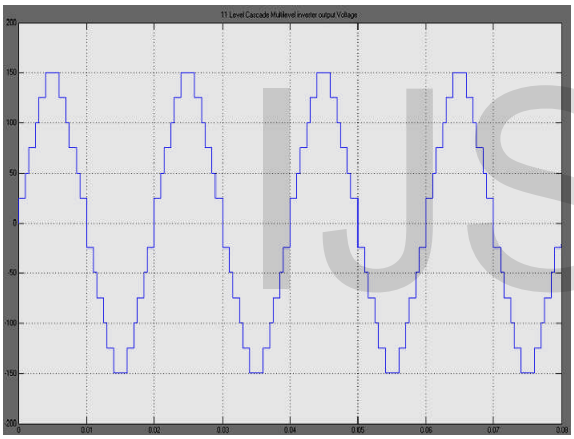


Figure 47 MATLAB Model Single Phase Inverter



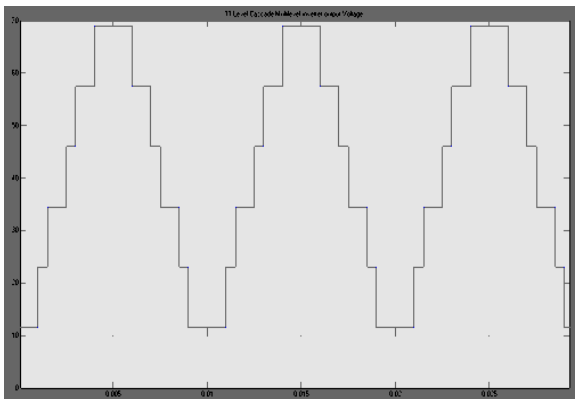
4.4.5. Simulation Result of 11 Levels CMLI

Figure 4.8 Simulation Results of 11 Levels CMLI



4.4.6. Level Positive Half Wave Output

Figure 4.9 11 level stepped output waveform



5. CONCLUSION

The disturbances in power electronics equipment are often periodic and rich in higher harmonics. They have been frequencies and are often above the bandwidth of regulators used to control fundamental components. Therefore the 'regular' control can only partially reduce their effects on the distortion of control variables. The cascade multilevel inverter with unequal DC sources is illustrated and the gate triggering pulse is given by the step modulation Genetic algorithms technique.

In this project, the calculation time is insensitive to the switching frequency ratio and the stepped wave form had minimal total harmonic distortion. The fifth and seventh order harmonics are reduced by using the harmonic elimination method. The algorithms was able to efficiency eliminate fifth and seventh harmonics from the line current. for the fast convergences it was found to filter out fundamental components and use only the remaining signal(higher harmonic – distorted current) for adaptation. A simulation was performed to show the output of proposed method.

6. REFERENCES

[1] .Harmonic Elimination of Cascade Multilevel Inverters with Unequal DC Sources Using Particle Swarm Optimization by H. Taghizadeh and M. Tarafdar Hagh, Member, IEEE, IEEE Transactions on Industrial Electronics, Vol. 57, NO. 11, November 2010

[2] .Cheng Y, Qian C, Crow M L , Pekarek S , and Atcitty S, "A comparison of diode- clamped and cascaded multilevel converters for a STATCOM with energy storage," IEEE Trans. Ind. Electron., vol. 53, no. 5, pp. 1512– 1521, Oct. 2006.

[3] .Chiasson J N, Tolbert L M,. McKenzieK J, and Du Z, "Real-time computer control of a multilevel converter using the mathematical theory of resultant," Math. Comput. Simul., vol. 63, no. 3– 5, pp. 197– 208, 2003.

[4] .Chiasson J N, Tolbert L M, Mc KenzieK J, and Du Z,, "The use of power sums to solve the harmonic elimination equations for multilevel converters," EPE J., vol. 15, no. 1, pp. 19– 27, Feb. 2005.

[5] .Clerc M and Kennedy J, "The particle swarm: Explosion, stability and Convergence in a multi – dimensional complex space," IEEE Trans. Evol. Comput., vol. 2, no. 3, pp. 91– 96, Jun. 1998.

[6] .Enjeti P N, Ziogas P D , and Lindsay J L, "Programmed PWM Techniques to eliminate harmonics: A critical evaluation," IEEE Trans. Ind. Appl., vol. 26, no. 2, pp. 302– 316, Mar./Apr. 1990.

[7] .Ozpineci E, Tolbert M , and Chiasson L M, "Harmonic optimization of multilevel converters using genetic algorithms," IEEE Power Electron. Lett., vol. 3, no. 3, pp. 92– 95, Sep. 2005.

[8] Patel H S and Hoft R G , "Generalized harmonic elimination and voltage control in thyristor inverters: Part I — Harmonic elimination," IEEE Trans. Ind. Appl., vol. IA-9, no. 3, pp. 310– 317, May/Jun. 1973.

[9] Carrasco. DJ., Franquelo LG , Bialasiewicz J.T Galvan "Power-electronic systems for the grid integration of renewable energy sources: A survey," IEEE Trans. Ind. Electron., vol. 53, no. 4, pp. 1002– 1016, Jun. 2006.

[10] L. M. Tolbert, J. N. Chiasson, K. McKenzie, and Z. Du, "Elimination of harmonics in a multilevel converter with non equal DC sources," in Proc. IEEE Appl. Power Electron. Conf., Miami, FL, Feb. 9– 13, 2003,pp. 589– 595.

[11] J. Kennedy and R. Eberhart, Swarm Intelligence. San Mateo, CA:Morgan Kaufmann, 2001.

[12] Y. Liu, H. Hong, and A. Q. Huang, "Real-time algorithm for minimizing THD in multilevel inverters with unequal or varying voltage steps under staircase modulation," IEEE Trans. Ind. Electron., vol. 56, no. 6, pp. 2249– 2258, Jun. 2009.

[13] J. Rodríguez, J. Lai, and F. Peng, "Multilevel inverters: A survey of topologies, controls and applications," IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 724– 738, Aug. 2002

[14] P. W. Hammond, "A new approach to enhance power quality for medium voltage AC drives," IEEE Trans. Ind. Appl., vol. 33, no. 1, pp. 202– 208,
Jan/Feb. 1997